

Fig. 1

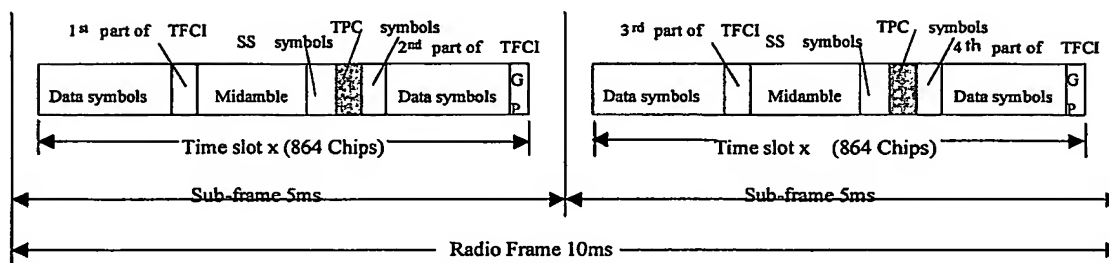


Fig. 2

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| Slot Format # | Spreading Factor | Midamble length (chips) | N _{TPCI} (bits) | N _{SS} & N _{TPC} (bits) | Bits/slot | N _{Data/Slot} (bits) | N _{data/field(1)} (bits) | N _{data/field(2)} (bits) |
|---------------------|---------------------|-------------------------------|-----------------------------|--|-----------|----------------------------------|--------------------------------------|--------------------------------------|
| 0 | 16 | 144 | 0 | 0 & 0 | 88 | 88 | 44 | 44 |
| 1 | 16 | 144 | 4 | 0 & 0 | 88 | 86 | 42 | 44 |
| 2 | 16 | 144 | 8 | 0 & 0 | 88 | 84 | 42 | 42 |
| 3 | 16 | 144 | 16 | 0 & 0 | 88 | 80 | 40 | 40 |
| 4 | 16 | 144 | 32 | 0 & 0 | 88 | 72 | 36 | 36 |
| 5 | 16 | 144 | 0 | 2 & 2 | 88 | 84 | 44 | 40 |
| 6 | 16 | 144 | 4 | 2 & 2 | 88 | 82 | 42 | 40 |
| 7 | 16 | 144 | 8 | 2 & 2 | 88 | 80 | 42 | 38 |
| 8 | 16 | 144 | 16 | 2 & 2 | 88 | 76 | 40 | 36 |
| 9 | 16 | 144 | 32 | 2 & 2 | 88 | 68 | 36 | 32 |
| 10 | 1 | 144 | 0 | 0 & 0 | 1408 | 1408 | 704 | 704 |
| 11 | 1 | 144 | 4 | 0 & 0 | 1408 | 1406 | 702 | 704 |
| 12 | 1 | 144 | 8 | 0 & 0 | 1408 | 1404 | 702 | 702 |
| 13 | 1 | 144 | 16 | 0 & 0 | 1408 | 1400 | 700 | 700 |
| 14 | 1 | 144 | 32 | 0 & 0 | 1408 | 1392 | 696 | 696 |
| 15 | 1 | 144 | 0 | 2 & 2 | 1408 | 1404 | 704 | 700 |
| 16 | 1 | 144 | 4 | 2 & 2 | 1408 | 1402 | 702 | 700 |
| 17 | 1 | 144 | 8 | 2 & 2 | 1408 | 1400 | 702 | 698 |
| 18 | 1 | 144 | 16 | 2 & 2 | 1408 | 1396 | 700 | 696 |
| 19 | 1 | 144 | 32 | 2 & 2 | 1408 | 1388 | 696 | 692 |
| 20 | 1 | 144 | 0 | 32 & 32 | 1408 | 1344 | 704 | 640 |
| 21 | 1 | 144 | 4 | 32 & 32 | 1408 | 1342 | 702 | 640 |
| 22 | 1 | 144 | 8 | 32 & 32 | 1408 | 1340 | 702 | 638 |
| 23 | 1 | 144 | 16 | 32 & 32 | 1408 | 1336 | 700 | 636 |
| 24 | 1 | 144 | 32 | 32 & 32 | 1408 | 1328 | 696 | 632 |

Fig. 3

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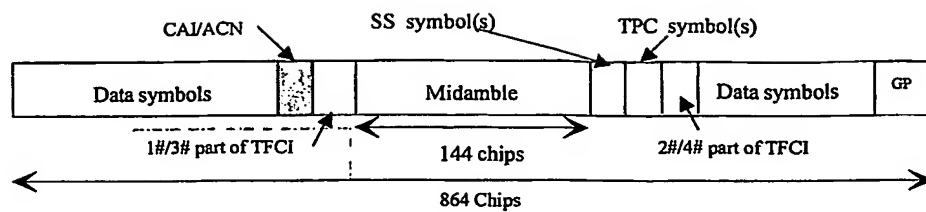


Fig. 4

| Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
|---------|---------|---------|---------|---------|---------|--------|--------|
| Code 15 | Code 14 | Code 13 | Code 12 | Code 11 | Code 10 | Code 9 | Code 8 |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Code 7 | Code 6 | Code 5 | Code 4 | Code 3 | Code 2 | Code 1 | Code 0 |

Fig. 5

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| Slot Format# | Spreading Factor | Midamble length (chips) | N_{cal} (bits) | N_{FEC} (bits) | $N_{\text{SS}} \& N_{\text{TPC}}$ (bits) | Bits/slot | $N_{\text{Data/Slot}}$ (bits) | $N_{\text{Data/Mod(1)}}$ (bits) | $N_{\text{Data/Mod(2)}}$ (bits) |
|-----------------|---------------------|----------------------------|----------------------------|----------------------------|---|-----------|----------------------------------|------------------------------------|------------------------------------|
| 0 | 16 | 144 | 0 | 0 | 0 & 0 | 88 | 88 | 44 | 44 |
| 0 | 16 | 144 | 16 | 0 | 0 & 0 | 88 | 88 | 28 | 44 |
| 1 | 16 | 144 | 0 | 4 | 0 & 0 | 88 | 86 | 42 | 44 |
| 1 | 16 | 144 | 16 | 4 | 0 & 0 | 88 | 86 | 26 | 44 |
| 2 | 16 | 144 | 0 | 8 | 0 & 0 | 88 | 84 | 42 | 42 |
| 2 | 16 | 144 | 16 | 8 | 0 & 0 | 88 | 84 | 26 | 42 |
| 3 | 16 | 144 | 0 | 16 | 0 & 0 | 88 | 80 | 40 | 40 |
| 3 | 16 | 144 | 16 | 16 | 0 & 0 | 88 | 80 | 24 | 40 |
| 4 | 16 | 144 | 0 | 32 | 0 & 0 | 88 | 72 | 36 | 36 |
| 4 | 16 | 144 | 16 | 32 | 0 & 0 | 88 | 72 | 20 | 36 |
| 5 | 16 | 144 | 0 | 0 | 2 & 2 | 88 | 84 | 44 | 40 |
| 5 | 16 | 144 | 16 | 0 | 2 & 2 | 88 | 84 | 28 | 40 |
| 6 | 16 | 144 | 0 | 4 | 2 & 2 | 88 | 82 | 42 | 40 |
| 6 | 16 | 144 | 16 | 4 | 2 & 2 | 88 | 82 | 26 | 40 |
| 7 | 16 | 144 | 0 | 8 | 2 & 2 | 88 | 80 | 42 | 38 |
| 7 | 16 | 144 | 16 | 8 | 2 & 2 | 88 | 80 | 26 | 38 |
| 8 | 16 | 144 | 0 | 16 | 2 & 2 | 88 | 76 | 40 | 36 |
| 8 | 16 | 144 | 16 | 16 | 2 & 2 | 88 | 76 | 24 | 36 |
| 9 | 16 | 144 | 0 | 32 | 2 & 2 | 88 | 68 | 36 | 32 |
| 9 | 16 | 144 | 16 | 32 | 2 & 2 | 88 | 68 | 20 | 32 |
| 10 | 1 | 144 | 0 | 0 | 0 & 0 | 1408 | 1408 | 704 | 704 |
| 11 | 1 | 144 | 0 | 4 | 0 & 0 | 1408 | 1406 | 702 | 704 |
| 12 | 1 | 144 | 0 | 8 | 0 & 0 | 1408 | 1404 | 702 | 702 |
| 13 | 1 | 144 | 0 | 16 | 0 & 0 | 1408 | 1400 | 700 | 700 |
| 14 | 1 | 144 | 0 | 32 | 0 & 0 | 1408 | 1392 | 696 | 696 |
| 15 | 1 | 144 | 0 | 0 | 2 & 2 | 1408 | 1404 | 704 | 700 |
| 16 | 1 | 144 | 0 | 4 | 2 & 2 | 1408 | 1402 | 702 | 700 |
| 17 | 1 | 144 | 0 | 8 | 2 & 2 | 1408 | 1400 | 702 | 698 |
| 18 | 1 | 144 | 0 | 16 | 2 & 2 | 1408 | 1396 | 700 | 696 |
| 19 | 1 | 144 | 0 | 32 | 2 & 2 | 1408 | 1388 | 696 | 692 |
| 20 | 1 | 144 | 0 | 0 | 32 & 32 | 1408 | 1344 | 704 | 640 |
| 21 | 1 | 144 | 0 | 4 | 32 & 32 | 1408 | 1342 | 702 | 640 |
| 22 | 1 | 144 | 0 | 8 | 32 & 32 | 1408 | 1340 | 702 | 638 |
| 23 | 1 | 144 | 0 | 16 | 32 & 32 | 1408 | 1336 | 700 | 636 |
| 24 | 1 | 144 | 0 | 32 | 32 & 32 | 1408 | 1328 | 696 | 632 |

Fig. 6

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| Bit3 | Bit2 | Bit1 | Bit0 | User number |
|------|------|------|------|-------------|
| 1 | 1 | 1 | 1 | 16 |
| 1 | 1 | 1 | 0 | 15 |
| 1 | 1 | 0 | 1 | 14 |
| 1 | 1 | 0 | 0 | 13 |
| 1 | 1 | 0 | 1 | 12 |
| 1 | 1 | 0 | 0 | 11 |
| 1 | 0 | 0 | 1 | 10 |
| 1 | 0 | 0 | 0 | 9 |
| 0 | 1 | 1 | 1 | 7 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 1 | 1 |

Fig. 7

| Slot Format# | Spreading Factor | Midamble length (chips) | N _{AC} (bits) | N _{TFCI} (bits) | N _{SS} & N _{TPC} (bits) | Bits /slot | N _{data/slot} (bits) | N _{data/field} (1) (bits) | N _{data/field} (2) (bits) |
|-----------------|---------------------|-------------------------------|---------------------------|-----------------------------|---|---------------|----------------------------------|---------------------------------------|---------------------------------------|
| 0 | 16 | 144 | 0 | 0 | 0 & 0 | 88 | 88 | 44 | 44 |
| 1 | 16 | 144 | 4 | 4 | 0 & 0 | 88 | 86 | 42 | 44 |
| 2 | 16 | 144 | 0 | 8 | 0 & 0 | 88 | 84 | 42 | 42 |
| 3 | 16 | 144 | 0 | 16 | 0 & 0 | 88 | 80 | 40 | 40 |
| 4 | 16 | 144 | 0 | 32 | 0 & 0 | 88 | 72 | 36 | 36 |
| 5 | 16 | 144 | 0 | 0 | 2 & 2 | 88 | 84 | 44 | 40 |
| 6 | 16 | 144 | 4 | 4 | 2 & 2 | 88 | 82 | 42 | 40 |
| 7 | 16 | 144 | 0 | 8 | 2 & 2 | 88 | 80 | 42 | 38 |
| 8 | 16 | 144 | 0 | 16 | 2 & 2 | 88 | 76 | 40 | 36 |
| 9 | 16 | 144 | 0 | 32 | 2 & 2 | 88 | 68 | 36 | 32 |
| 10 | 1 | 144 | 0 | 0 | 0 & 0 | 1408 | 1408 | 704 | 704 |
| 11 | 1 | 144 | 0 | 4 | 0 & 0 | 1408 | 1406 | 702 | 704 |
| 12 | 1 | 144 | 0 | 8 | 0 & 0 | 1408 | 1404 | 702 | 702 |
| 13 | 1 | 144 | 0 | 16 | 0 & 0 | 1408 | 1400 | 700 | 700 |
| 14 | 1 | 144 | 0 | 32 | 0 & 0 | 1408 | 1392 | 696 | 696 |
| 15 | 1 | 144 | 0 | 0 | 2 & 2 | 1408 | 1404 | 704 | 700 |
| 16 | 1 | 144 | 0 | 4 | 2 & 2 | 1408 | 1402 | 702 | 700 |
| 17 | 1 | 144 | 0 | 8 | 2 & 2 | 1408 | 1400 | 702 | 698 |
| 18 | 1 | 144 | 0 | 16 | 2 & 2 | 1408 | 1396 | 700 | 696 |
| 19 | 1 | 144 | 0 | 32 | 2 & 2 | 1408 | 1388 | 696 | 692 |
| 20 | 1 | 144 | 0 | 0 | 32 & 32 | 1408 | 1344 | 704 | 640 |
| 21 | 1 | 144 | 0 | 4 | 32 & 32 | 1408 | 1342 | 702 | 640 |
| 22 | 1 | 144 | 0 | 8 | 32 & 32 | 1408 | 1340 | 702 | 638 |
| 23 | 1 | 144 | 0 | 16 | 32 & 32 | 1408 | 1336 | 700 | 636 |
| 24 | 1 | 144 | 0 | 32 | 32 & 32 | 1408 | 1328 | 696 | 632 |

Fig. 8

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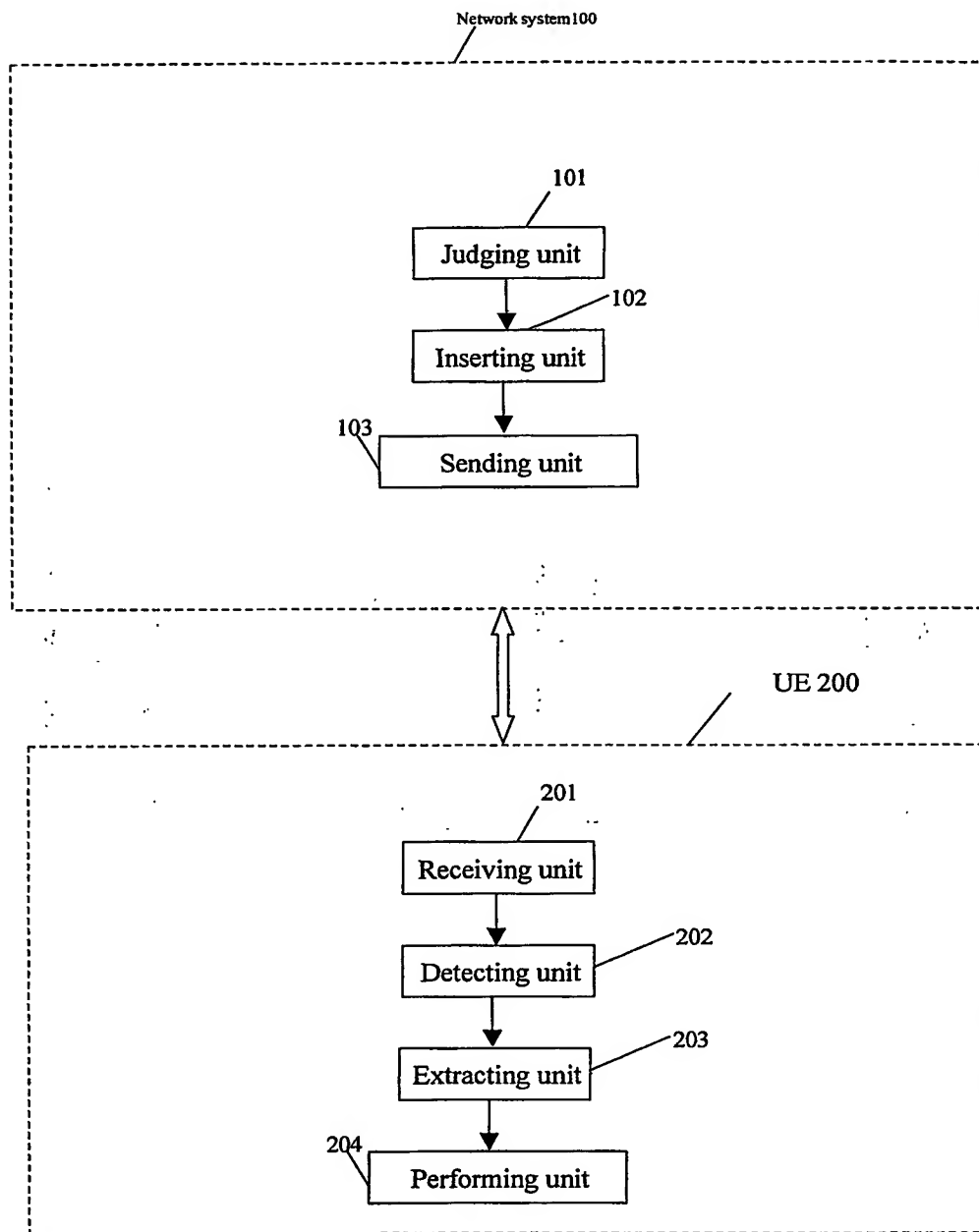


Fig.9

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